Srikant Bharadwaj

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Redmond, WA

Systems researcher with 6 years of industrial research experience in the field of GPU architecture, high-performance computing, performance analysis and modeling, power modeling, and quantum computing.

Professional Experience

Microsoft Apr 2022 - Present
Senior Researcher (Full-Time) Redmond, WA

- Innovations in hardware-software codesign for Office 365 and Azure.

Advanced Micro Devices, Research Feb 2018 – Apr 2022
Senior Design Researcher (Full-Time) Bellevue, WA

- Research in architecting GPUs, CPUs, and accelerators for efficient high-performance computation used for scientific computing and machine learning workloads.
- Transferred technology to commercial products which led to the development of **fastest supercomputers**, Frontier (ORNL) and El Capitan (LLNL).
- Optimizing CPU and GPU architectures for modern machine intelligence workloads and frameworks: Pytorch, TensorFlow, DeepBench, DNNMark, etc.
- Developed quantum and cryogenic software/firmware support infrastructure for AMD CPUs and GPUs.
- Designed and developed detailed interconnect models for accurate and high-fidelity simulations (Open sourced as HeteroGarnet in gem5).
- Earned ***Spotlight Awards*** for contributions to internal GPU power modelling infrastructure.

Apple Inc. May 2017 – Aug 2017
iOS GPU Design (Intern) Cupertino, CA

- Designed a tracking scheme for GPU kernel crashes in iPhones and iPads during heavy graphics usages.
- Architected software-based mechanism which improves productivity of engineers when fixing remote problems occurred during the usage of commercial devices.

NVIDIA Graphics Jan 2016 – July 2016
ASIC Engineer II (Full-Time), Integrated GPU Design Bangalore, India

- Designed and implemented the client-side support for VCS Save restore mechanism for integrated GPU in Tegra which saved 78% of test run times.
- Contributed with a software team to upgrade a software based headless (no-CPU) fullchip testing system for new Tegra chips which simulated CPU+GPU fullchip tests.

Oracle Systems Jul 2014 – Jan 2016
Associate Software Engineer (Full-Time), R&D Team, Oracle Systems Bangalore, India

- Designed and implemented a way to import virtualized operating system instances into a cluster.
- Researched on timings of server failure by creating an algorithm for convergence of server down times.

ST Microelectronics Jan 2014 – Jun 2014
Intern, IP Design and Verification (Intern), Automotive Product Group Noida, India

- Developed a simulation environment for the subsystem using Specman *e* and Verilog.
- Analyzed the RTL regression results and used HDL code coverage and functional coverage to measure the exhaustiveness.

Education

Ph.D. Electrical and Computer Engineering	**Georgia Institute of Technology, GA, USA** Thesis: Heterogeneous Network-on-Chip Architectures GPA: 4.00/4.00	Dec 2017 – Dec 2022 (Expected)
M.S. Electrical and Computer Engineering	**Georgia Institute of Technology, GA, USA** Thesis: Scalable Translation Lookup Buffer Architectures GPA: 4.00/4.00	Aug 2016 – Dec 2017
B.E. (Hons.) Electrical and Electronics Engineering	**BITS Pilani, India** Electrical and Electronics Engineering GPA: 8.32/10	Aug 2010 – May 2014

Selected Publications

Scalable Distributed Shared Last-Level TLBs Using Low-Latency Interconnects (MICRO) Oct 2018
Srikant Bharadwaj, Guilherme Cox, Tushar Krishna, Abhishek Bhattacharjee

Optimizing GPU Cache Policies for Machine Learning Workloads (IISWC, arxiv) Nov 2019
John Alsop, Matthew Sinclair, Srikant Bharadwaj, et al.

Kite: A Family of Heterogeneous Interposer Topologies Enabled via Accurate Interconnect Modeling (DAC) Feb 2020
Srikant Bharadwaj, Jieming Yin, Brad Beckmann, Tushar Krishna

The gem5 simulator: Version 20.0+ (arxiv) Jul 2020
J Lowe-Power, Srikant Bharadwaj, et al.

DUB: Dynamic Underclocking and Bypassing in Network-on-Chip for Heterogeneous GPU Workloads (NOCS) Oct 2021
Srikant Bharadwaj, Shomit Das, Yasuko Eckert, Mark Oskin, Tushar Krishna

Accelerating Variational Quantum Algorithms Using Circuit Concurrency May 2021
Salonik Resch, Anthony Gutierrez, Srikant Bharadwaj, Yasuko Eckert, Mark Oskin, Gabriel Loh

Predict; Don't React for Enabling Efficient Fine-Grain DVFS in GPUs Jan 2022
Srikant Bharadwaj, Shomit Das, Brad Beckmann, Kaushik Mazumdar, Steve Kosonocky

Application-Aware Reconfiguration of High Bandwidth Memory in GPUs May 2021
Max Ruttenberg, Srikant Bharadwaj, Anthony Gutierrez, Yasuko Eckert, Mark Oskin

Scaling Address Translation in multi-core architectures Dec 2017
Srikant Bharadwaj, Tushar Krishna
Georgia Institute of Technology Thesis

Importing a zone into zone-cluster configuration Jan 2016
Srikant Bharadwaj, Srivatsa BR, Mahesh Kumar
Oracle Yearly Proceedings

Books

Interconnect Modeling for Homogeneous and Heterogeneous Multiprocessors Springer
Srikant Bharadwaj, Tushar Krishna
Network-on-Chip Security and Privacy

Public Service

- Official maintainer of gem5 simulator (github.com/gem5/gem5/)
- Open sourced gem5 GPU and HeteroGarnet models.
- Committee reviewer at academic computer architecture conferences (MASCOTS, ISCA)
- Hosted tutorials in top tier computer architecture conferences (ISCA)
- Active participation in academic computer architecture conferences (ISCA, MICRO, PACT, DAC, etc.)

Selected Patents

Routing Flits in a Network-on-Chip based on Operating States of Routers (Granted)
Srikant Bharadwaj, Shomit Das. Application No.: 16/188900
Credit Based Flow Control Mechanism for Use in Multiple Link Width Interconnect Systems (Granted)
Srikant Bharadwaj. Application No.: 16/271371
Dynamic Voltage Frequency Scaling Based on Active Memory Barriers (Filed)
Srikant Bharadwaj. Application No.: 16/425414
Compiler Directed Fine-Grained Power Management (Filed)
Srikant Bharadwaj et al. Application No.: 17/033000
Dynamically configurable overprovisioned microprocessor (Filed)
Srikant Bharadwaj et al. Application No.: 17/037727
Spatial distribution of DRAM pages with combined timing parameter tuning (Filed)
Srikant Bharadwaj et al.
Application aware dynamic tuning of DRAM parameters by leveraging thermal headroom (Filed)
Srikant Bharadwaj et al.

Selected Academic Projects

Intel GPU Architecture Analytical Modelling Aug 2016 – Dec 2016

Advisor: Dr. Hyesoon Kim, Georgia Institute of Technology

- Investigating architecture for analyzing performance bottlenecks of parallel applications in CPU + GPU systems.
- Developing an analytical model for estimating the execution time of massive parallel programs.
- Developing micro-benchmarks in OpenCL to be used for ensuring accuracy in the analytical model.

Digital String Tuner Aug 2013 – Dec 2013

Funded by Texas Instruments, India for Analog Design Competition

- Designed and implemented a standalone guitar tuner using Piccolo Microcontroller.
- Reached the pre-final round of the contest and was shortlisted in the top innovative designs.

Achievements and Awards

- Received a scholarship from Angiras Foundation, USA for academic performance.
- Nominated for '**Rookie of the year'** award at Oracle for the year 2014 for co-implementing a way to import instances of running Solaris instances to another cluster.
- Earned '**Spotlight Award**' at AMD for contributions to internal GPU power modelling infrastructure.

Extracurricular Activities

- President of Visual Effects Club, Students' Union, 2012-13, BITS Pilani Hyderabad Campus.
- Technical Representative of Electrical Department, Placement Division, BITS Pilani Hyderabad, 2013-14.
- Member of Recreational Activity Forum, 2011-12, a college body taking care of recreational activities on campus.

References

- **Dr. Tushar Krishna**
  Associate Professor, Georgia Institute of Technology
  tushar@ece.gatech.edu

- **Dr. Matthew Sinclair**
  Assistant Professor, University of Wisconsin-Madison
  sinclair@cs.wisc.edu